Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples, and further ~~comprises~~comprising control means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, and wherein the delay sub-lines are directly ~~line is~~ coupled to a plurality of multiplexers for providing early, in-time, and late outputs.

2. (previously presented) A receiver as claimed in claim 1, characterized in that the delay line comprises a single series of delay sub-lines.

3. (previously presented) A receiver as claimed in claim 1, characterized in that the delay line comprises various series of delay sub-lines.

4. (previously presented) A receiver as claimed in claim 1, characterized in that a delay sub-line is accessible with a frequency twice as fast as the samples of an input signal received by the receiver.

5. (previously presented) A receiver as claimed in claim 1, characterized in that one memory area is associated to one delay sub-line.

6. (previously presented) A receiver as claimed in claim 1, characterized in that the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines.

7. (previously presented) A receiver as claimed in claim 1, characterized in that the read addresses of the samples of a series of samples are situated at addresses immediately adjacent or equal to one another.

8. (previously presented) A receiver as claimed in claim 3, characterized in that two series of samples are read in parallel.

9. (previously presented) A receiver as claimed in the preceding claim 8, characterized in that the delay line comprises selection means of a series of delay sub-lines to which belongs one of the two series of samples read as a function of the delay.

10. (previously presented) A receiver as claimed in claim 1, characterized in that the delay line comprises a position factor indicating the position of a reference sample from a series of samples of an input signal in the series of delay sub-lines to which it belongs.

11. (previously presented) A receiver as claimed in the preceding claim 8, characterized in that the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines,

so that the memory areas for a series of samples read are identical for each equal position factor value.

12. (currently amended) A delay line for delaying an input signal, said input signal comprising a series of samples, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples, and in that the delay line comprises control means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays, and wherein the delay sub-lines are directly ~~line is~~ coupled to a plurality of multiplexers for providing early, in-time, and late outputs.

13. (currently amended) A method of delaying an input signal by means of a delay line, said input signal comprising a series of samples, characterized in that it comprises the steps of:

dividing the delay line into a series of delay sub-lines each configured to receive a sample from the series of samples of the input signal, each of the delay sub-lines including a memory area to receive the sample, said delay line being configured to delay said input signal by a series of delays, [[and]]

generating read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input

signal and a delay expressed as a number of sampling periods of the series of delays, and

directly coupling the delay sub-lines ~~line~~ to a plurality of multiplexers for providing early, in-time, and late outputs.

14. (previously presented) A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples, and further comprises control means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, wherein the delay line comprises various series of delay sub-lines, two series of samples are read in parallel, and the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value.